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EXAMINER	
HE, AMY	
ART UNIT	PAPER NUMBER
2831	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,545	ARGUELLES ET AL.	
	Examiner	Art Unit	
	AMY HE	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-12* is/are allowed.

6)☒ Claim(s) *1-4,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kakizawa et al. (U. S. Pub. No. 2005/0146346).

As for claim 1, Kakizawa et al. discloses (in Figs. 1 and 2) a test switching circuit (DFT circuitry in Figs. 1 and 2, including transistors 190, 192 and 290, 292) for a high speed data interface of an integrated circuit comprising a plurality of switching transistors(e.g. 190, 192 in Fig. 1 and 290, 292 in Fig. 2) which switch in a test mode an integrated termination resistor (132 and 134 in Fig. 1) output stage coupled to an output pad (110, 112 in Fig. 1) of said integrated circuit in a data transmission signal path to an integrated termination resistor (260, 262 in Fig. 2) input stage coupled to an input pad (210,212 in Fig. 2) of said integrated circuit in a data reception signal path, wherein said plurality of switching transistors provide for a plurality of internal test signal

paths between said input pad and said output pad (the analog loop back path, see [0015], [0016], [0018], [0021]).

As for claims 13 and 14, Kakizawa et al. discloses an integrated circuit having high speed data interface comprising:

a transmitting signal path (in Fig. 1) for transmitting data via a data transmission line which is connected through an output pad (110, 112) to an integrated termination resistor (132, 134) output stage coupled to the output pad in said data transmission signal path, wherein the integrated termination resistor (132, 134) output stage is provided for adapting the output impedance of said data transmission signal path to a load connected to said transmission data line through the output pad(110, 112);

a reception data signal path (see Fig. 2) for receiving data via a data reception line, which is connected through an input pad (210, 212) to an integrated termination resistor (260, 262) input stage coupled to the input pad in said data reception signal path, wherein the integrated termination resistor (260, 262) input stage is provided for adapting the input impedance of said data reception signal path to a load connected to said reception data line through the input pad; and

a controllable test switching circuit (DFT circuitry in Figs. 1 and 2, including transistors 190, 192 and 290, 292) comprising a plurality of switching transistors(e.g. 190, 192 in Fig. 1 and 290, 292 in Fig. 2) for switch in a test mode the integrated termination resistor (132 and 134 in Fig. 1) output stage to the integrated termination resistor input stage (260, 262 in Fig. 2) to form an internal feedback test loop (the analog loop back path, see [0015]) within said integrated circuit, wherein said plurality of

switching transistors provide for a plurality of internal test signal paths between said input pad and said output pad (the analog loop back path, see [0015], [0016], [0018], [0021]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakizawa et al. (U. S. Pub. No. 2005/0146346), in view of Gandini et al. (U. S. Patent No. 5, 197,083).

As for claim 2, Kakizawa et al. discloses the test switching circuit according to claim 1 as discussed above. Kakizawa et al. does not specifically disclose that the test switching circuit is connected to a configuration register.

It is conventional in the art to use a configuration register to control and configure transmitter and receiver according to the different operating or test modes, as evidenced in Gandini et al. (col. 11, lines 25-34).

A person of ordinary skill in the art would find it obvious at the time the invention was made to modify Kakizawa et al. to use a conventional configuration register, as taught by Gandini et al. for configuring and controlling the switching test circuitry

according to the different operating or test modes (see [0033] in Kakizawa et al. and col. 11, lines 25-34 in Gandini et al.).

3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakizawa et al. (U. S. Pub. No. 2005/0146346), in view of applicant's admitted prior art (thereafter referred to as AAP)(see the prior art figure 3 in the instant application)

As for claims 3 and 4, Kakizawa et al. discloses that the termination resistor output and input stages comprise variable resistors (132, 134, 260, 262). Kakizawa et al. does not specifically disclose that the termination resistor output and input stages are programmable.

However, it is conventional in the art to use programmable termination resistor output stage and input stage, as evidenced in AAP (see Fig 3.)

A person of ordinary skill in the art would find it obvious at the time the invention was made to modify Kakizawa et al. to replace the variable termination resistors with the conventional programmable termination resistors as taught in AAP, for the purpose of obtaining a greater range of impedance matching with the load connected to the termination resistor output stage and the input stage.

Allowable Subject Matter

4. Claims 5-12 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Claims 5-12 are allowable because none of the prior art discloses or fairly suggest a test switching circuit for a high speed data interface of an integrated circuit

comprising: a second transistor connected between a first transistor and a reference potential node; a third transistor connected between the reference potential node and a sixth transistor; a fourth transistor connected between the first transistor and a test node; a fifth transistor connected between the test node and the sixth transistor; wherein the six transistor is connected to the termination resistor input stage of the data reception signal path.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments filed March 18, 2009 have been fully considered but they are not persuasive.

In response to applicant's argument that "Kakizawa does not disclose or suggest an integrated termination resistor output stage that can be switched to an output pad", it is noted that the features upon which applicant relies (i.e., an integrated termination resistor output stage that can be **switched to an output pad**) are not recited in the rejected claim(s). According to claims 1, 13 and 14, the claims recite a plurality of switching transistors which switch an integrated termination resistor output stage coupled to an output pad **to an integrated termination resistor input stage** (not to the output pad as argued by the applicant). Although the claims are interpreted in light of

the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that "Kakizawa again fails to disclose or suggest switching transistors for switching an input pad to an integrated termination resistor input stage", it is noted that the features upon which applicant relies (i.e., switching **an input pad** to an integrated termination resistor input stage) are not recited in the rejected claim(s). According to claims 1, 13 and 14, the claims recites a plurality of switching transistors which switch **an integrated termination resistor output stage** (not an input pad as argued by applicant) to an integrated termination resistor input stage coupled to an input pad. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that Kakizawa teach one single loop back path, or that Kakizawa does not teach a plurality of switching transistors for providing a plurality of internal test signal paths, the examiner asserts that Kakizawa does indeed disclose a plurality of switching transistors (190, 192, 290, 292) for providing a plurality of internal test signal paths (i.e. two paths: one loop back path 199 controlled by transistors 190 and 192, and another loop back path 299 controlled by transistors 290 and 292).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HE whose telephone number is (571)272-2230. The examiner can normally be reached on 9:30am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amy He/
Examiner, Art Unit 2831